



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/518,182

06/20/2005

Paul R Routley

30740/285902

3530

4743

7590

08/13/2008

MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER

MANDEVILLE, JASON M

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

08/13/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/518,182	Applicant(s) ROUTLEY ET AL.	
	Examiner JASON M. MANDEVILLE	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4,7,10,13,14,17,23,27,28 and 30-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4,7,10,13,14,17,23,27,28 and 30-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 December 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 February 2008 has been entered.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A

COMPACT DISC.

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1, 4, 7, 10, 14, 17, 23, 27, 28, and 31** are rejected under 35 U.S.C.

103(a) as being unpatentable over Yamazaki et al. (hereinafter "Yamazaki" US 6,424,326) in view of Sakamoto (US 5,594,463).

5. As pertaining to **Claim 1**, Yamazaki discloses (see Fig. 1, Fig. 3, Fig. 4, and Fig. 6) a display driver (see Fig. 1) for an active matrix electroluminescent display (see

Col. 1, Ln. 8-26 and Ln. 34-38), the display comprising a plurality of electroluminescent pixels (104; see Fig. 3) each pixel (104) comprising a pixel driver circuit (see Fig. 3; also see Col. 5, Ln. 29-67 through Col. 6, Ln. 1-7), each pixel driver circuit (see Fig. 3) including a drive field effect transistor (131) having a gate connection for driving the associated pixel (104) in accordance with a voltage (V) on the gate connection (see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48), the display driver (see Fig. 3) comprising:

a plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator) each for driving a row or column of the display with an adjustable constant current determining the voltage on the gate connection of the pixel driver circuit (see (131); also see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48);

a display element brightness controller (see (136, 135, 134) of Fig. 3 in conjunction with Fig. 6) configured to control the plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator; see Fig. 3) to drive the gate connections (see (131) of Fig. 3) to control the electroluminescent output from the pixels (104; see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

a current sensor (136; see Fig. 3) to sense a current on the gate connection (see (131) in Fig. 3; also see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

a power controller (206; see Fig. 6) coupled to the current sensor (136; see Fig. 3) for controlling an adjustable voltage power supply (V; see Fig. 3) to the plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator; again, see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14; also see Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48).

Yamazaki does not explicitly disclose a voltage sensor to sense the voltage on the gate connection; and a power controller coupled to the voltage sensor for controlling an adjustable voltage power supply to the plurality of adjustable constant current generators, the power controller being configured to reduce the power supply voltage in response to the sensed voltage to a point where a voltage of the adjustable voltage power supply is just sufficient for the adjustable constant current generator with a highest output current to be able to provide a highest gate connection voltage, the highest gate connection voltage being determined by the highest output current in accordance with a compliance of the adjustable constant current generator with the highest output current.

However, Sakamoto discloses (see Fig. 1, Fig. 2, and Fig. 6) a display driver for a matrix electroluminescent display (see Col. 1, Ln. 12-21), the display comprising a plurality of electroluminescent pixels(i.e., (14) in Fig. 1 corresponding to (52) in Fig. 6), each pixel comprising a pixel driver circuit (see Fig. 1 and Fig. 6), the display driver comprising: a plurality of adjustable constant current generators (see (10) in Fig. 1

corresponding to (32) in Fig. 6) each for driving a row or column of the display with an adjustable constant current (see Col. 1, Ln. 63-67 through Col. 2, Ln. 1-57); a display element brightness controller (see (+V, 10) in Fig. 1 corresponding to (32) in Fig. 6) configured to control the plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6) to control the electroluminescent output from the pixels (Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8). Further, Sakamoto discloses a voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) to sense the voltage on the driver; and a power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) coupled to the voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) for controlling an adjustable voltage power supply (i.e., (+V)) to the plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6; also see Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8 and Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61), the power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) being configured to reduce the power supply voltage (+V) in response to the sensed voltage (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) to a point where a voltage of the adjustable voltage power supply (+V) is just sufficient for the adjustable constant current generator (see (10) in Fig. 1 corresponding to (32) in Fig. 6) with a highest output current to be able to provide a highest driving voltage (again, see Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61), the highest driving voltage being determined by the highest output current in accordance with a compliance of the adjustable constant current generator (see (10) in Fig. 1 corresponding to (32) in Fig. 6) with the highest output current (i.e., the driving voltage is

reduced to the minimum limit necessary for driving the electroluminescent element; see Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61; also see Col. 2, Ln. 18-28).

Yamazaki and Sakamoto both disclose a means of driving an electroluminescent display by controlling an adjustable power supply to an adjustable constant current generator. Further, the inventions of Yamazaki and Sakamoto are in the same field of endeavor. Further, Sakamoto discloses a means of reducing the power consumption in the electroluminescent display by reducing the power supply voltage to a display element (see Col. 1, Ln. 32-62). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Yamazaki with the teachings of Sakamoto. Further, it would have been obvious to one of ordinary skill in the art that in the combined invention of Yamazaki and Sakamoto, the voltage sensor disclosed by Sakamoto would be applied to sense the voltage on the gate connection disclosed by Yamazaki, as the gate connection determines the driving voltage.

6. As pertaining to **Claim 4**, Yamazaki and Sakamoto both disclose (see Fig. 3 of Yamazaki and see Fig. 1 and Fig. 6 of Sakamoto) that the voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6 of Sakamoto) is configured to sense the voltage on a gate connection (see (131) in Fig. 3 of Yamazaki) by sensing the voltage on an electrode of the display (i.e., see Fig. 6 of Sakamoto).

7. As pertaining to **Claim 7**, Yamazaki discloses (see Fig. 3) that a pixel (104) includes a photodiode (136), and wherein a photocurrent through the photodiode (136) is determined by an adjustable constant current to determine a brightness of the pixel (see Abstract and see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14).

8. As pertaining to **Claim 10**, both Yamazaki and Sakamoto discloses that the highest output current is provided to a pixel having a maximum brightness relative to others of the pixels (i.e., the highest output current implicitly determines the maximum brightness; see Abstract and see Col. 15, Ln. 31-39; Col. 29, Ln. 40-48; and Col. 11, Ln. 46-63 of Yamazaki; and see Col. 2, Ln. 58-67 through Col. 3, Ln. 1-14 of Sakamoto).

9. As pertaining to **Claim 14**, both Yamazaki and Sakamoto disclose (see Fig. 6 of Yamazaki and see Fig. 1 and Fig. 6 of Sakamoto) the adjustable voltage power supply (see (206) in Fig. 6 of Yamazaki; and see (+V) in Fig. 1 of Sakamoto).

10. As pertaining to **Claim 17**, Yamazaki discloses (see Fig. 1, Fig. 3, Fig. 4, and Fig. 6) a method of operating an active matrix electroluminescent display (see Col. 1, Ln. 8-26 and Ln. 34-38), the display comprising a plurality of pixels (104; see Fig. 3) each pixel (104) comprising an associated pixel driver circuit (see Fig. 3; also see Col. 5, Ln. 29-67 through Col. 6, Ln. 1-7), each pixel driver circuit (see Fig. 3) including

Art Unit: 2629

a drive field effect transistor (131) having a gate connection for driving the associated display element (104) in accordance with a voltage (V) on the gate connection (see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48), the display (see Fig. 3) having a plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator) each for driving a row or column of the display with an adjustable constant current determining the voltage on the gate connection (see (131); also see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48), an adjustable voltage power supply (see (206) in Fig. 6) to the plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator), and a plurality of control lines (V, G, S) for setting the brightness of each pixel (104; see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14), the method comprising:

controlling (see (136, 135, 134) of Fig. 3 in conjunction with Fig. 6) the plurality of adjustable constant current generators (i.e., driving transistor (131) and power supply (V) comprise an adjustable constant current generator; see Fig. 3) to drive the gate connections (see (131) of Fig. 3) to set the brightness of pixels (104) of the display using the control lines (V, G, S; see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

monitoring (see (136) in Fig. 3) control lines (V, G, S) of the display to sense the current on the gate connections (see (131) in Fig. 3; also see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

controlling (206; see Fig. 6) the power supply voltage (V; see Fig. 3) responsive to the monitoring (see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14; also see Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48).

Yamazaki does not explicitly disclose monitoring control lines of the display to sense the voltages on the gate connections; reducing the power supply voltage responsive to the monitoring to a point where a voltage of the adjustable voltage power supply is just sufficient for the adjustable constant current generator with a highest output current to be able to provide a highest gate connection voltage, the highest gate connection voltage being determined by the highest output current in accordance with a compliance of the adjustable constant current generator with the highest output current.

However, Sakamoto discloses (see Fig. 1, Fig. 2, and Fig. 6) a display driver and method for a matrix electroluminescent display (see Col. 1, Ln. 12-21), the display comprising a plurality of electroluminescent pixels(i.e., (14) in Fig. 1 corresponding to (52) in Fig. 6), each pixel comprising a pixel driver circuit (see Fig. 1 and Fig. 6), the display driver comprising: a plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6) each for driving a row or column of the display with an adjustable constant current (see Col. 1, Ln. 63-67 through Col. 2, Ln. 1-57); a display element brightness controller (see (+V, 10) in Fig. 1 corresponding to (32) in Fig.

6) configured to control the plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6) to control the electroluminescent output from the pixels (Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8). Further, Sakamoto discloses a voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) to sense the voltage on the control lines; and a power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) coupled to the voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) for controlling an adjustable voltage power supply (i.e., (+V)) to the plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6; also see Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8 and Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61), the power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) being configured to reduce the power supply voltage (+V) in response to the sensed voltage (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) to a point where a voltage of the adjustable voltage power supply (+V) is just sufficient for the adjustable constant current generator (see (10) in Fig. 1 corresponding to (32) in Fig. 6) with a highest output current to be able to provide a highest driving voltage (again, see Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61), the highest driving voltage being determined by the highest output current in accordance with a compliance of the adjustable constant current generator (see (10) in Fig. 1 corresponding to (32) in Fig. 6) with the highest output current (i.e., the driving voltage is reduced to the minimum limit necessary for driving the electroluminescent element; see Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61; also see Col. 2, Ln. 18-28).

Yamazaki and Sakamoto both disclose a means of driving an electroluminescent display by controlling an adjustable power supply to an adjustable constant current generator. Further, the inventions of Yamazaki and Sakamoto are in the same field of endeavor. Further, Sakamoto discloses a means of reducing the power consumption in the electroluminescent display by reducing the power supply voltage to a display element (see Col. 1, Ln. 32-62). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Yamazaki with the teachings of Sakamoto. Further, it would have been obvious to one of ordinary skill in the art that in the combined invention of Yamazaki and Sakamoto, the monitoring (i.e., voltage sensing) disclosed by Sakamoto would be applied to monitor (i.e., sense) the voltage on the gate connection disclosed by Yamazaki, as the gate connection determines the driving voltage.

11. As pertaining to **Claim 23**, Yamazaki discloses (see Fig. 3) that a pixel (104) includes a photodiode (136), and wherein a current through the photodiode (136) is determined by an adjustable constant current (see Abstract and see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14).

12. As pertaining to **Claim 27**, Yamazaki discloses an active matrix display driver configured to operate in accordance with the method of **Claim 17** (see Col. 1, Ln. 8-14).

13. As pertaining to **Claim 28**, Yamazaki discloses that the electroluminescent display can comprise an organic light emitting diode display (see Col. 1, Ln. 34-38).

14. As pertaining to **Claim 31**, Yamazaki discloses that the electroluminescent display can comprise an organic light emitting diode display (see Col. 1, Ln. 34-38).

15. **Claims 13, 30, 32, and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Sakamoto and further in view of Applicant Admitted Prior Art (hereinafter "APA").

16. As pertaining to **Claim 13**, both Yamazaki and Sakamoto disclose (see Fig. 6 and Fig. 3 of Yamazaki and see Fig. 1 and Fig. 6 of Sakamoto) that the power controller (see (206) in Fig. 6 of Yamazaki and see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6 of Sakamoto) is further configured to increase the power supply voltage when the gate connection voltage (as disclosed by Yamazaki) of the brightest pixel has not reduced to less than a threshold value after a predetermined interval (i.e., when the gate connection voltage of the brightest pixel has not reduced to less than an arbitrary threshold value, such as the transistor threshold value, after any arbitrary predetermined interval, such as a frame period, a reset period, etc.; see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14 of Yamazaki; and see Col. 2, Ln. 29-34; Col. 4, Ln. 56-65 of Sakamoto).

17. As pertaining to **Claim 30**, Yamazaki discloses that the electroluminescent display can comprise an organic light emitting diode display (see Col. 1, Ln. 34-38).

18. As pertaining to **Claim 32**, Yamazaki discloses (see Fig. 1, Fig. 3, Fig. 4, and Fig. 6) a display driver (see Fig. 1) for an active matrix electroluminescent display (see Col. 1, Ln. 8-26 and Ln. 34-38), the display comprising a plurality of electroluminescent pixels (104; see Fig. 3) each comprising a pixel driver circuit (see Fig. 3; also see Col. 5, Ln. 29-67 through Col. 6, Ln. 1-7), each pixel driver circuit (see Fig. 3) including a drive field effect transistor (131) having a gate connection for driving the associated display element (104) in accordance with a voltage (V) on the gate connection (see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48) and a capacitor (133) coupled across the gate connection and a photodiode (136; see Fig. 3) to control the gate connection voltage (V) in accordance with the brightness of the pixel (see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48), the display configured for cyclical driving (i.e., the display having a driving cycle; see Fig. 5), the gate connection voltage gradually decaying (i.e., the capacitor voltage implicitly decays over time) according to the brightness of the associated pixel (104; again, see Col. 6, Ln. 18-67 through Col. 7, Ln. 1-52 in conjunction with Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48) the display driver (see Fig. 3) comprising:

a display element brightness controller (see (136, 135, 134) of Fig. 3 in conjunction with Fig. 6) to cyclically drive the display and configured to provide an output to drive a gate connection (see (131) of Fig. 3) to control the electroluminescent output from the pixels (104; see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

a current sensor (136; see Fig. 3) to sense a current on the gate connection (see (131) in Fig. 3; also see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14);

a power controller (206; see Fig. 6) coupled to the current sensor (136; see Fig. 3) for controlling an adjustable voltage power supply (V; see Fig. 3) to provide and adjustable voltage (V) to the electroluminescent display to power the drive transistors (131) for driving the pixels (104), the power controller being configured to control the power supply (V; again, see Col. 11, Ln. 46-63 in conjunction with Col. 12, Ln. 6-67 through Col. 13, Ln. 1-14; also see Col. 15, Ln. 31-39 and Col. 29, Ln. 40-48).

Yamazaki does not explicitly disclose a voltage sensor to sense the voltage on the gate connection; and a power controller coupled to the voltage sensor for controlling an adjustable voltage power supply to provide an adjustable voltage to the electroluminescent display to power the drive transistors for driving the pixels, the power controller being configured to reduce the power supply voltage in response to the sensed voltage such that the gate connection voltage of a brightest pixel has decayed sufficiently to switch the brightest pixel off at the end of a driving cycle of the display.

However, Sakamoto discloses (see Fig. 1, Fig. 2, and Fig. 6) a display driver for a matrix electroluminescent display (see Col. 1, Ln. 12-21), the display comprising a plurality of electroluminescent pixels (i.e., (14) in Fig. 1 corresponding to (52) in Fig. 6), each pixel comprising a pixel driver circuit (see Fig. 1 and Fig. 6), the display driver comprising: a plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6) each for driving a row or column of the display with an adjustable constant current (see Col. 1, Ln. 63-67 through Col. 2, Ln. 1-57); a display element brightness controller (see (+V, 10) in Fig. 1 corresponding to (32) in Fig. 6) configured to control the plurality of adjustable constant current generators (see (10) in Fig. 1 corresponding to (32) in Fig. 6) to control the electroluminescent output from the pixels (Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8). Further, Sakamoto discloses a voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) to sense the voltage on the driver; and a power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) coupled to the voltage sensor (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) for controlling an adjustable voltage power supply (i.e., (+V)) to provide an adjustable voltage (+V) to the electroluminescent display for driving the pixels (see Col. 4, Ln. 29-67 through Col. 5, Ln. 1-8 and Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61), the power controller (see (+V, CPU 54) in Fig. 1 corresponding to (32, CPU 54) in Fig. 6) being configured to reduce the power supply voltage (+V) in response to the sensed voltage (see (18) in Fig. 1 corresponding to (Terminal A) in Fig. 6) such that the voltage of a brightest pixel has decayed sufficiently to switch the brightest pixel off at the end of a driving cycle of the display (i.e., the power controller is

configured to reduce the power supply voltage (+V) to any voltage; for example, the power controller can reduce the power supply voltage (+V) such that the voltage of a brightest pixel has decayed sufficiently to switch the brightest pixel off at the end of a driving cycle; further, it is implicit that at the end of a driving cycle, the voltage of all of the pixels can be allowed to decay sufficiently to switch off; see Col. 6, Ln. 22-67 through Col. 7, Ln. 1-61; also see Col. 2, Ln. 18-28).

Yamazaki and Sakamoto both disclose a means of driving an electroluminescent display by controlling an adjustable power supply to an adjustable constant current generator. Further, the inventions of Yamazaki and Sakamoto are in the same field of endeavor. Further, Sakamoto discloses a means of reducing the power consumption in the electroluminescent display by reducing the power supply voltage to a display element (see Col. 1, Ln. 32-62). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Yamazaki with the teachings of Sakamoto. Further, it would have been obvious to one of ordinary skill in the art that in the combined invention of Yamazaki and Sakamoto, the voltage sensor disclosed by Sakamoto would be applied to sense the voltage on the gate connection as disclosed by Yamazaki, as the gate connection determines the driving voltage.

Neither Yamazaki nor Sakamoto explicitly disclose a photodiode coupled across the capacitor to reduce the gate connection voltage in accordance with the brightness of the pixel. However, APA discloses (see Fig. 2b) a display driver for an active matrix

electroluminescent display wherein a capacitor (258) is coupled to a gate connection (see (256)) and a photodiode (266) is coupled across the capacitor to reduce the gate connection voltage in accordance with the brightness of the pixel and wherein a gate connection voltage gradually decays by a current flow through the photodiode (266; see Page 5, Para. [2] through Page 6, Para. [1]). The inventions of Yamazaki, Sakamoto, and APA are in the same field of endeavor. Further, APA discloses an alternate arrangement to Yamazaki for providing optical feedback in an electroluminescent display. Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Yamazaki and Sakamoto with the teachings of APA.

19. As pertaining to **Claim 33**, both Yamazaki and Sakamoto disclose (see Fig. 6 of Yamazaki and see Fig. 1 and Fig. 6 of Sakamoto) the adjustable voltage power supply (see (206) in Fig. 6 of Yamazaki; and see (+V) in Fig. 1 of Sakamoto).

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inukai (US 2002 / 0101395) discloses a means of adjusting power supply voltage based on current sensed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. MANDEVILLE whose telephone number is 571-270-3136. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason Mandeville
Examiner
Art Unit 2629

/J. M. M./
Examiner, Art Unit 2629

/Alexander Eisen/
Supervisory Patent Examiner, Art Unit 2629